

## OP-QSFP-DD-SR8

### 400G QSFP-DD SR8 Transceiver SR8 MPO-16

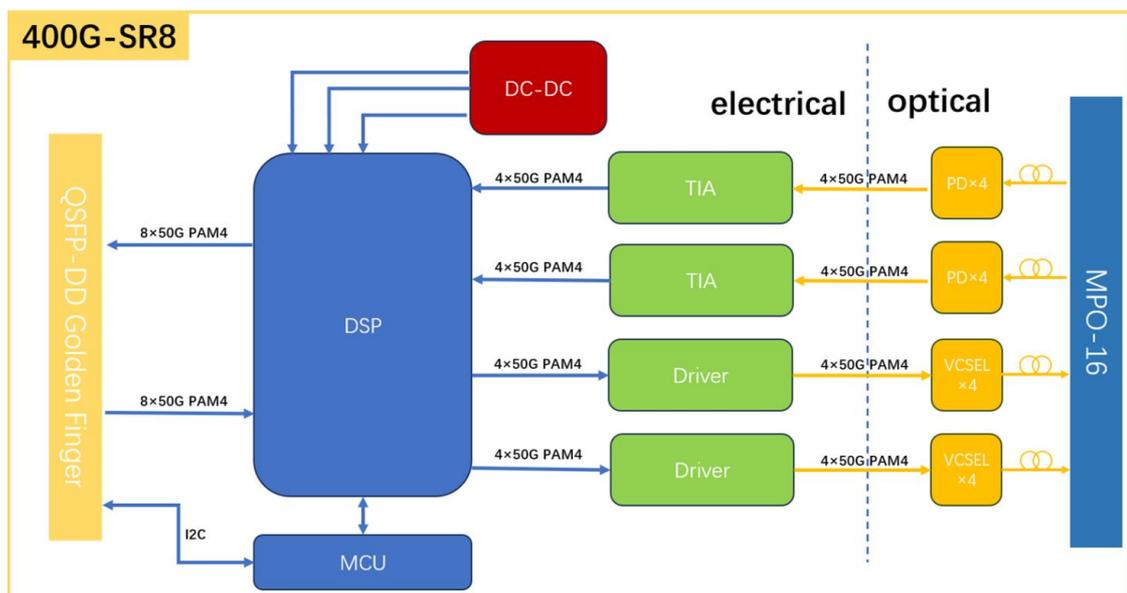
#### Features

- ◆ QSFP-DD Serial Optical Interface
  - 8x50G PAM4 retimed 400GAUI-8 electrical interface
  - MPO-16 APC connector
  - 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
  - Maximum link length of 70m on OM3 or 100m on OM4
  
- ◆ QSFP-DD MSA Compliant
  - Hot Pluggable QSFP-DD form factor
  - Compliant with CMIS 4.0
  
- ◆ Support Protocol
  - Compliant with IEEE 802.3cm
  
- ◆ Low Power Consumption
  - Less than 9W in temperature range of 0 to 70°C

#### Applications

- ◆ 400GBASE-SR8 400G Ethernet
- ◆ Data center

#### Functional Block Diagram



## 1. General Description

OP-QSFPDD-SR8 is an Eight-Channel, Parallel, Pluggable, Fiber-Optic QSFP-DD for 400Gigabit Ethernet applications. This transceiver is a high performance module for short-range data communication and interconnect application. It integrates eight data lanes in each direction with 8x26.5625GBd. The length of QSFP-DD SR8 is up to 70 meters over OM3 MMF or 100 meters over OM4 MMF. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm.

## 2. Absolute Maximum Ratings and Recommended Operating Conditions

**Table 2.1 Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	° C
Case Operating Temperature	Top	0	70	° C
Relative Humidity (non-condensation)	RH		85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

**Table 2.2 Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	° C
Relative Humidity(non-condensing)	RH	5	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc	-	9	W
Bit Rate	BR		425	Gbps
Fiber Length on OM3 MMF			70	m
Fiber Length on OM4 MMF			100	m

### 3. Optical Specification

#### 3.1 Optical Transmitter

**Table 3.1 Transmitter Optical Interface**

Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	DR		26.5625		Gbd
Modulation format		PAM4			
Center Wavelength	$\lambda$	840	850	860	nm
RMS spectral width	$\sigma$			0.6	nm
Average Launch power, each lane	$P_{avg}$	-6.5		4	dBm
Optical Power OMA, each Lane	$P_{OMA}$	-4.5		3	dBm
Launch power in OMAouter minus TDECQ		-5.9			dBm
Transmitter and dispersion eye closure (TDECQ), each lane	TDECQ			4.5	dB
Extinction ratio	ER	3			dB
Optical Return Loss Tolerance	ORLT			12	dB
Optical Power for TX DISABLE				-30	dBm

#### 3.2 Optical Receiver

**Table 3.2 Receiver Optical Interface**

Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	BR		26.5625		Gbd
Modulation format		PAM4			
Center Wavelength	$\lambda$	840	850	860	nm
Damage threshold		5			dBm
Average receive power, each lane		-8.4		4	dBm
Receiver reflectance	Rr			-12	dB
Receiver sensitivity, each lane <sup>1</sup>		RS = max (-6 , SECQ - 7.9)			dBm
Stressed receiver sensitivity, each lane				-3.4	dBm
Rx LOS	Assert		-30		dBm
	De-assert			-9	dBm
	Hysteresis		0.5		dB

Notes:



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1. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

## 4. Electrical Specification

Table 4.1 High speed Electrical Specifications

Parameters	Min	Typical	Max	Unit
Supply voltage	3.135		3.465	V
Supply Current			2.59	A
Input differential impedance	90	100	110	$\Omega$
Differential data input swing			880	mVpp
Differential data output swing			900	mVpp
Bit Error Rate			2.4E-4	
Input Logic Level High	2		Vcc	V
Input Logic Level Low	0		0.8	V
Output Logic Level High	Vcc-0.5		Vcc	V
Output Logic Level Low	0		0.4	V

## Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

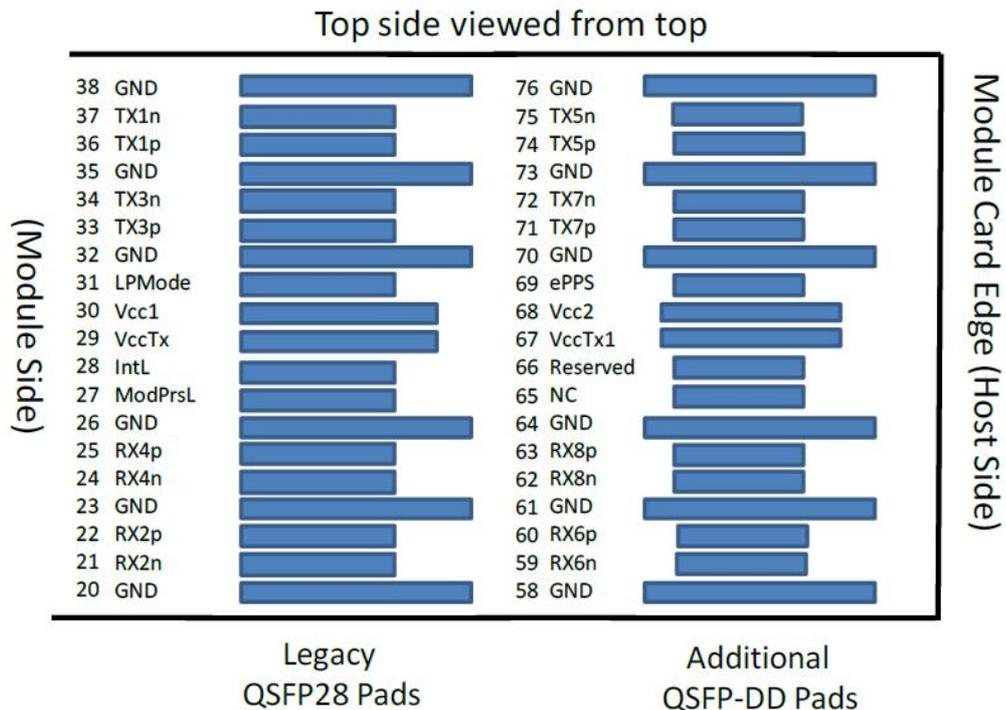
**Table 5.2 Digital Diagnostic Monitor Accuracy**

Parameter	Accuracy	Unit
Internally measured transceiver temperature	+/-3	° C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power	+/-3	dB
Measured Rx received average optical power	+/-3	dB

## 6. Pin Assignment and Description

### 6.1 PIN Definitions

QSFP-DD Transceiver Pad Layout, host PCB QSFP-DD Pinout, and PIN Descriptions are as follows:



### Bottom side viewed from bottom

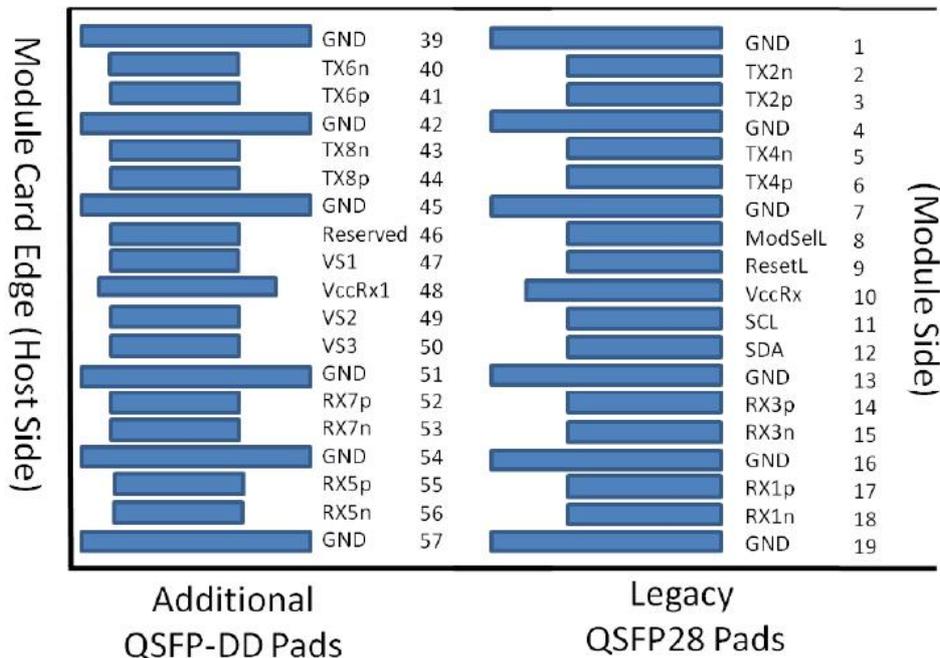


Figure 6.1 QSFP-DD Transceiver Electrical Pad Layout

## 6.2 PIN Description

Table 6.2 Pin Description

Pin	Name	Logic	Description	Power Seq	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVC MOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVC MOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	



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15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMODE	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3



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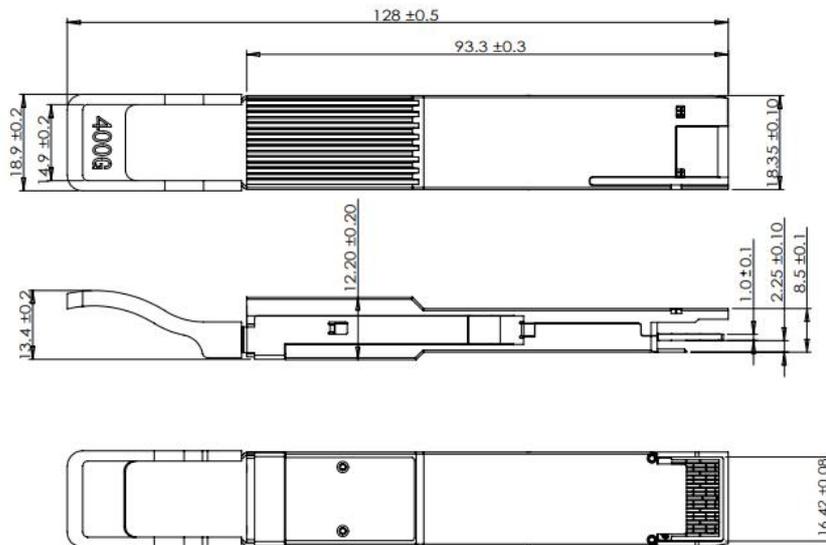
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reserved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

## 7. Mechanical Dimensions

Below shows the package dimensions of the module. Package dimensions are specified in QSFP-DD MSA.



## 8. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E
OP-QSFPDD-SR8	0 to 70°C	100m	MMF	VCSEL 850nm	PIN